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TITLE

INPUT/OUTPUT BUFFER

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an input/output buffer, and more particularly, to an input/output buffer capable of occupying reduced wafer area.

Description of the Related Art

Conventionally, most IC devices are driven by a system voltage in the range of 0-5V. In these IC devices, the high-voltage logic signals are therefore set at the system voltage and the low-voltage logic signals are set at the ground voltage. With advances in semiconductor technology, however, the system voltage can be now reduced to 3.3V because the gate oxide layers in the IC device are thinner. Still lower system voltage may be possible in the future. In practice, however, an New 3.3V IC device is usually used in conjunction with some older 5V peripheral devices. For instance, an New 3.3V VGA (video graphic adapter) IC may be used in conjunction with other older 5V peripheral devices in a personal computer. Compatibility between the new 3.3V devices and the older 5V devices can thus be a problem.

FIG. 1 is a schematic circuit diagram showing the circuit structure of a conventional I/O buffer 14 used in a 3.3V IC device. As shown, the I/O buffer 14 is coupled to an input buffer 16 and an I/O pad 20 of an IC device. The I/O buffer 14 is composed of a first circuit 10, a second circuit 12, a PMOS transistor P1, and an NMOS transistor N1. When the I/O

buffer operates in input mode, both the PMOS transistor P1 and the NMOS transistor N1 must be switched to a non-conducting state. To do this, the first circuit 10 outputs a high-voltage signal, for example 3.3V, to the gate of the PMOS transistor P1, thereby switching the PMOS transistor P1 to a non-conducting state. Meanwhile, the second circuit 12 outputs a low-voltage signal, for example 0V, to the gate of the NMOS transistor N1, thereby switching the NMOS transistor N1 to a non-conducting state.

However, if the I/O pad 20 receives a 5V input logic signal, it subjects the PMOS transistor P1 a gate voltage of 3.3V, a drain voltage of 5V, and a source voltage of 3.3V. Since the gate voltage (3.3 V) is lower than the drain voltage (5 V) at the PMOS transistor P1, the gate voltage switches the PMOS transistor P1 to a reverse conducting state. Moreover, since the PMOS transistor P1 is formed on N-type substrate and its source and drain are both P-type, a PN junction diode is formed between its drain and the N-well. Furthermore, since the drain of the PMOS transistor P1 is connected to the I/O pad 20, now receiving the 5 V input logic signal, higher than the 3.3V system voltage, and the substrate thereof is connected to the 3.3V system voltage, the PN junction diode is subjected to a forward bias, causing an undesired large current to flow between the external 5V source and the internal 3.3V source.

As a solution, an improved I/O buffer for the 3.3V IC is disclosed. FIG. 2 is a schematic diagram showing an I/O buffer capable of accepting an input logic signal voltage higher than the system voltage. The P-gate control circuit 32 conveys the first gate control signal Vp to the PMOS

transistor Q3 of the I/O circuit. The N-well control circuit 34 adjusts the voltage at the floating N-well of the PMOS transistor Q3 according to the input voltage at the I/O pad 36. Undesired current leakage is thus prevented. In this I/O buffer, however, transistors Q5 and Q6 are required to follow design rule for electrostatic discharge (ESD) protection because the transistors Q5 and Q6 of the P-gate control circuit 32 are connected to the I/O pad 36 directly. Thus, it occupies a larger wafer area.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to protect I/O buffer from undesired current leakage when accepting an input logic signal voltage higher than the system voltage.

According to the above mentioned object, the present invention provides an I/O buffer capable of occupying reduced wafer area.

In the I/O buffer of the present invention, an input/output circuit has a first PMOS transistor, and a first NMOS transistor. The input/output circuit has an I/O pot coupled to an I/O pad. The first PMOS transistor has a N-well region, a gate receiving a first gate control signal, and a drain serving as the I/O port. A N-well control circuit controls the voltage level at the N-well region of the first PMOS transistor according to the input signals at the I/O pad. A P-gate control circuit receives a second gate control signal and outputs to the gate of the first PMOS transistor. The P-gate control circuit is composed of a transmission gate and a third PMOS transistor. The transmission gate and the third

PMOS transistor do not follow the design rule for ESD, and the required wafer area for P-gate control circuit can be decreased because the P-gate control circuit is not directly connected to the I/O pad.

When the I/O buffer operates in input mode, if the input signal to the transmission terminal is 5V higher than the system voltage of 3.3V, the N-well control circuit 130 adjusts the voltage level at the N-well region of the first PMOS transistor to the voltage level of 5V. When the voltage state at the transmission terminal is switched from 5V to 0V, lower than the system voltage of 3.3V, the N-well control circuit adjusts the voltage level at the N-well region of the first PMOS transistor to the voltage level of the system voltage (3.3 V). Thus, undesired current leakage is prevented.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention can be more fully understood by the subsequent detailed description and examples with reference made to the accompanying drawings, wherein:

Fig. 1 is a diagram of a conventional input/output buffer;

FIG 2 is a schematic diagram showing a conventional I/O buffer capable of accepting an input logic signal voltage higher than the system voltage;

Fig. 3 is a schematic diagram showing the circuit structure of the I/O buffer according to the present invention; and

Fig. 4 shows a circuit with a plurality of PMOS drivers according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Fig. 3 is a schematic diagram showing the circuit structure of the I/O buffer according to the present invention. This I/O buffer 100 is capable of accepting an input logic signal higher than the system voltage VCC. In the following embodiment of the present invention, the system voltage VCC is 3.3V, and the input logic signal switches between 0V and 5V, wherein the 5V high-voltage logic state is higher than the system voltage VCC of 3.3V. However, it is to be understood that the invention is not limited to this embodiment.

As shown in Fig. 3, the I/O buffer 100 has an I/O circuit 140, a P-gate control circuit 120 and a N-well control circuit 130. The I/O buffer 100 is connected to an I/O pad 110 of the IC device (not shown) through an I/O port 132. The operating of the I/O buffer 100 is controlled by two gate control signals PG and NG from the core circuit (not shown).

In this embodiment, the I/O circuit 140 is composed of a PMOS transistor P1 and two NMOS transistors N1 and N2. In the I/O circuit 140, the PMOS transistor P1 has a source coupled to the system voltage VCC, a drain coupled to the I/O pad through the I/O port 132, and a floating N-well region VNW. The NMOS transistor N1 has a gate coupled to the first gate control single NG from the core circuit (not shown), a source coupled to the ground. The NMOS transistor N2 has a gate coupled to the system voltage VCC, a drain coupled to the I/O pad through the I/O port 132, and a source coupled to the drain of the NMOS transistor N1.

In this embodiment, the P-gate control circuit 120 is composed of a transmission gate and a PMOS transistor P6, wherein the transmission gate has a NMOS transistor N4 and a PMOS transistor P5. The P-gate control circuit 120 receives a second gate control signal PG from the core circuit (not shown) and outputs to the gate of the PMOS transistor P1.

In the P-gate control circuit 120, the PMOS transistor P6 has a gate coupled to the system voltage VCC, a source coupled to the floating N-well region of the PMOS transistor P1, and a drain coupled to the gate of the PMOS transistor P1. The PMOS transistor P5 has a source coupled to the second gate control signal PG, and a drain coupled to the gate of the PMOS transistor P1 and the drain of the PMOS transistor P6. The NMOS transistor N4 has a gate coupled to the system voltage VCC, a source coupled to the second gate control signal PG, and a drain coupled to the gate of the PMOS transistor P1.

In this embodiment, the N-well control circuit 130 is composed of three PMOS transistors P2~P4 and a NMOS transistor N3. The N-well control circuit 130 adjusts the voltage level at the floating N-well region VNW of the PMOS transistor P1 according to the input voltage at the I/O pad 110 when the I/O buffer 100 operates in input mode. In the N-well control circuit 130, the NMOS transistor N3 has a drain coupled to I/O pad 110, and a gate coupled the system voltage VCC. The PMOS transistor P2 has a source coupled to the I/O pad 110 through the I/O port 132, a gate coupled to the system voltage VCC, and a drain coupled to the floating N-well region VNW. The PMOS transistor P3 has a gate coupled to the system voltage VCC, a source coupled to the I/O pad 110 through the I/O port

132, and a drain coupled to the source of the NMOS transistor N3. The PMOS transistor P4 has a drain coupled to the system voltage VCC, a source coupled to the floating N-well region VNW, and a gate coupled to the source of the NMOS transistor N3 and the drain of the PMOS transistor P3. Furthermore, the floating N-well region VNW is connected to the substrate on which all PMOS transistors P1~P6 are formed.

When the I/O buffer 100 operates in input mode, the gate control signal NG is in a low-voltage state, and the NMOS transistor N1 is turned off. At the same time, the gate control signal PG is in a high-voltage state, and the PMOS transistor P1 is turned off. If the input signal to the I/O port 132 is 5V higher than the system voltage of 3.3V, it can be transferred into the floating N-well region VNW through the PMOS transistor P2 because the PMOS transistor P2 is now in a conducting state due to its gate voltage being connected to the 3.3V system voltage VCC lower than its drain voltage of 5V connected to the I/O port 132. Thus, the floating N-well region VNW is set at 5V. Furthermore, the PMOS transistor P3 is turned on also, the input signal of 5V is transferred into the gates of the PMOS transistors P4 and P5 through the PMOS transistor P3 and NMOS transistor N3, thus turning on the PMOS transistors P4 and P5. In addition, the PMOS transistor P6 is now in a conducting state due to its gate voltage being connected to the 3.3V system voltage VCC lower than its source voltage of 5V connected to the floating N-well VNW.

When the voltage state at the I/O port 132 is switched from 5V to 0V, the PMOS transistors P2 and P3 are both tuned off. Further, the input signal of 0V is transferred into the gate of the PMOS transistor P4 through the NMOS transistor

N3, thus turning on the PMOS transistor P4. As a result, the floating N-well is set at system voltage VCC. Undesired current leakage is thus prevented.

Therefore, the present invention can accept an input logic signal voltage higher than the system voltage, and prevent undesired current leakage. Further, in the present invention the transmission gate and the third PMOS transistor do not have to follow the design rule for electrostatic discharge (ESD) protection, and the wafer area required the for P-gate control circuit can be decreased because the P-gate control circuit is not directly connected to the I/O pad. Thus, it conserves wafer area.

Fig. 4 is another embodiment of the I/O buffer according to the present invention. In this case, the circuit 200 includes a plurality of PMOS drivers, each having a transmission gate and two corresponding PMOS transistors, wherein all drains of the PMOS transistors (P5_0~P5_N) are connected to the I/O pad 110. Further, each of the PMOS transistors (P4_0~P4_N) has a gate coupled to system voltage VCC, a source coupled to the floating N-well region VNW, and a drain coupled to the gate of the corresponding PMOS transistor. The PMOS transistors (P4_0~P4_N) do not have to follow the design rule for ESD protection because they are not connected to the I/O pad directly. Thus, when using a plurality of PMOS drives, wafer area conservation is more pronounced.

While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various

modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.